REMARKS

The above amendments to the above-captioned application along with the following remarks are being submitted as a full and complete response to the Official Action dated August 25, 2005. In view of the above amendments and the following remarks, the Examiner is respectfully requested to give due reconsideration to this application, to indicate the allowability of the claims, and to pass this case to issue.

Status of the Claims

Claims 4-10 and 12-15 are under consideration in this application. Claims 1-3 and 11 are being cancelled without prejudice or disclaimer. Claims 4-10 and 12-14 are being amended, as set forth above and in the attached marked-up presentation of the claim amendments, in order to more particularly define and distinctly claim Applicants' invention.

All the amendments to the claims are supported by the specification. Applicants hereby submit that no new matter is being introduced into the application through the submission of this response.

Formality Rejection

Claims 4-15 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. As such, the merits of these claims were not evaluated.

As indicated, the claims are being amended to distinguish between first control memories storing management information and second control memories storing storage structure information. Accordingly, the withdrawal of the outstanding informality rejection is in order, and is therefore respectfully solicited.

Prior Art Rejection

Claims 1-3 were rejected under 35 U.S.C. § 102(e) as being anticipated by US Pat. App. Pub. No. 2004/0083338 of Moriwaki et al. (hereinafter "Moriwaki"), and claim 1 was rejected as being anticipated by US Pat. App. Pub. No. 2003/0221070 of Minowa et al. (hereinafter "Minowa"). Claims 1-3 were further rejected under 35 U.S.C. § 103(a) as being unpatentable over US Pat. No. to 5,077,736 Dunphy et al. (hereinafter "Dunphy") in view of US Pat. No. 5,155,835 to Belsan (hereinafter "Belsan"). The prior art references of Fujimoto et al (2004/0153691), Okumoto et al. (2003/0204683), Abe et al. (6,385,114) and Cochran et

al. (2005/0097132) were cited as being pertinent to the present application. These rejections have been carefully considered, but are most respectfully traversed in view of the claims currently on file, as more fully discussed below.

The disk array device 10 of the invention (for example, the embodiment depicted in Fig. 1) comprising channel adapters 20 which control exchange of data with host apparatuses 1; disk adapters 30 which control exchange of data with storage devices 40; cache memory packages which are mounted with cache memories 50; first control memory packages 60A which are used by the channel adapters 20 and the disk adapters 30 and have first control memories 61A storing management information which is used for controlling the operation of the disk array device 10; and second control memory packages 60B which are used by the channel adapters 20 and the disk adapters 30 and have second control memories 61B storing storage structure information with regard to a storage structure of the cache memory 50 (p. 24, 2nd paragraph). The management information is stored in the first control memories 61A, respectively, and multiplexed, and at least one maintenance control unit which, in the case in which a failure has occurred in one of the second control memories 61B, restores the storage structure information stored in the second control memory 61B in which the failure has occurred. The maintenance control unit restores the storage structure information stored in the second control memory 61B, in which the failure has occurred, using a storage area of the first control memories 61A.

The invention recited in claim 12 (p. 28+) is directed to a maintenance method for the disk array device as now recited in claim 4, comprising: a failure detection step of detecting whether or not a failure has occurred in any one of the first control memories and the second control memories; anda maintenance step of, in the case in which a failure is detected, restoring information stored in one of the first control memories or one of the second control memories, in which the failure has occurred.

In particular, the maintenance step exclusively executes one of (1) a first maintenance mode which is executable in the case in which no usable free space exists in the first control memories, (2) a second maintenance mode which is executable in the case in which a usable free space exists a predetermined value or more in the first control memories, and (3) a third maintenance mode which is executable in the case in which a usable free space exists less than the predetermined value in the first control memories, and

(1) the first maintenance mode comprises the steps of:

(1-1) in the case in which a failure has occurred in the first control memory, if the first

control memory, in which the failure has occurred, has been replaced with a normal product, copying the management information multiplexed in the other first control memories to the replaced first control memory, and

(1-2) in the case in which a failure has occurred in the second control memory, reestablishing the storage structure information overwriting the storage structure information on the first control memory and,

if the second control memory, in which the failure has occurred, has been replaced with a normal product, reestablishing the storage structure information in the replaced second control memory, and

copying the management information multiplexed in the other first control memories to the first control memory on which the storage structure information has been overwritten,

(2) the second maintenance mode comprises the steps of:

(2-1) in the case in which a failure has occurred in the first control memory, if the first control memory, in which the failure has occurred, has been replaced with a normal product, copying the management information multiplexed in the other first control memories to the replaced first control memory, and

(2-2) in the case in which a failure has occurred in the second control memory, reestablishing the storage structure information in a free space of the first control memory, and permitting replacement of the second control memory, in which the failure has occurred, with a normal product, and

(3) the third maintenance mode comprises the steps of;

(3-1) in the case in which a failure has occurred in the first control memory, if the first control memory, in which the failure has occurred, has been replaced with a normal product, copying the management information multiplexed in the other first control memories to the replaced first control memory, and

(3-2) in the case in which a failure has occurred in the second control memory, partly reestablishing the storage structure information by a range which can be reestablished in a free space of the first control memory, and,

if the second control memory, in which the failure has occurred, has been replaced with a normal product, reestablishing a remaining part, which is not reestablished, of the storage structure information in the replaced second control memory.

Applicants respectfully submit that none of the cited prior art references teaches or

suggests "the storage structure information stored in the second control memory at fault being restored through the use of storage area in the first control memories storing management information" according to the invention.

Applicants contend that the cited references and their combinations all fail to teach or suggest each and every feature of the present invention as recited in independent claims 4 and 12. As such, the present invention as now claimed is distinguishable and thereby allowable over the rejections raised in the Office Action. The withdrawal of the outstanding prior art rejections is in order, and is respectfully solicited.

Conclusion

In view of all the above, clear and distinct differences as discussed exist between the present invention as now claimed and the prior art reference upon which the rejections in the Office Action rely, Applicants respectfully contend that the prior art references cannot anticipate the present invention or render the present invention obvious. Rather, the present invention as a whole is distinguishable, and thereby allowable over the prior art.

Favorable reconsideration of this application is respectfully solicited. Should there be any outstanding issues requiring discussion that would further the prosecution and allowance of the above-captioned application, the Examiner is invited to contact the Applicants' undersigned representative at the address and phone number indicated below.

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